HIGHLY SCALABLE GLITCH-FREE FREQUENCY DIVIDER

ABSTRACT

The present invention provides for a divider circuit for reducing anomalous output timing pulses. A latch is coupled to the division selection line. A comparator is coupled to the division selection line. A first synchronizer coupled to the output of the latch. A frequency divider is coupled to the output of the synchronizer. A second synchronizer is coupled to the output of the comparator and the output of the frequency divider. There is feedback between the output of the second synchronizer and the enable input of the latch, the reset of the first synchronizer, the reset of the second synchronized, and the reset of the divide by n divider.